ABSTRACT

The present invention includes a memory subsystem comprising at least two semiconductor devices, including at least one memory device, connected to a bus, where the bus includes a plurality of bus lines for carrying substantially all address, data and control information needed by said memory devices, where the control information includes device-select information and the bus has substantially fewer bus lines than the number of bits in a single address, and the bus carries device-select information without the need for separate device-select lines connected directly to individual devices.

The present invention also includes a protocol for master and slave devices to communicate on the bus and for registers in each device to differentiate each device and allow bus requests to be directed to a single or to all devices. The present invention includes modifications to prior-art devices to allow them to implement the new features of this invention. In a preferred implementation, 8 bus data lines and an AddressValid bus line carry address, data and control information for memory addresses up to 40 bits wide.

ABSTRACT OF THE DISCLOSURE

A method of controlling a memory device is disclosed wherein the memory device includes a plurality of memory cells. The method comprises providing first block size information to the memory device, wherein the first block size information defines a first amount of data to be output onto a bus in response to a read request. The method further includes issuing a first read request to the memory device, wherein in response to the first read request, the memory device outputs the first amount of data corresponding to the first block size information onto the bus synchronously with respect to an external clock signal. In one preferred embodiment, the method may include providing a code which is representative of a number of clock cycles of the first and second external clock which are to transpire before data is output by the memory device onto the bus. The memory device stores the code in a programmable register on the memory device. In this preferred embodiment, the first amount of data corresponding to the first block size information is output after the number of clock cycles of the external clock transpire.